

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

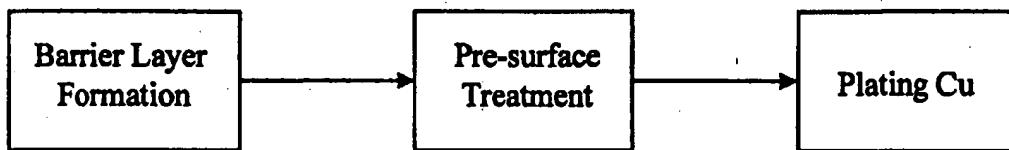


INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : C23C 18/18, C25D 5/34, H01L 21/288	A1	(11) International Publication Number: WO 99/53119 (43) International Publication Date: 21 October 1999 (21.10.99)
---	----	--

(21) International Application Number: PCT/US99/07906 (22) International Filing Date: 12 April 1999 (12.04.99) (30) Priority Data: 60/081,601 13 April 1998 (13.04.98) US (71) Applicant: ACM RESEARCH, INC [US/US]; 43236 Christy Street, Fremont, CA 94538 (US). (71)(72) Applicant and Inventor: WANG, Hui [-/US]; 38855 Litchfield Circle, Fremont, CA 94536 (US).	(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.
--	--

(54) Title: METHOD AND APPARATUS FOR ENHANCING ADHESION BETWEEN BARRIER LAYER AND METAL LAYER FORMED BY PLATING



(57) Abstract

An apparatus for plating conductive film on semiconductor wafer includes a stacked glue layer deposition chamber (310), a stacked pre-surface treatment chamber (312), five stacked plating baths (300, 302, 304, 306, 308), three stacked cleaning/dry chambers (314, 316, 318), robot (322), wafer cassette (321, 322), electrolyte tank (36) and plumbing box (330). The adhesion of metal plated directly on a barrier layer is enhanced by either pretreatment using plasma, ion irradiation, liquid or vapor phase etching by deposition of a glue layer, or by a combination thereof.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece	ML	Mali	TR	Turkey
BG	Bulgaria	HU	Hungary	MN	Mongolia	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MR	Mauritania	UA	Ukraine
BR	Brazil	IL	Israel	MW	Malawi	UG	Uganda
BY	Belarus	IS	Iceland	MX	Mexico	US	United States of America
CA	Canada	IT	Italy	NE	Niger	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NL	Netherlands	VN	Viet Nam
CG	Congo	KE	Kenya	NO	Norway	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NZ	New Zealand	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	PL	Poland		
CM	Cameroon	KR	Republic of Korea	PT	Portugal		
CN	China	KZ	Kazakhstan	RO	Romania		
CU	Cuba	LC	Saint Lucia	RU	Russian Federation		
CZ	Czech Republic	LI	Liechtenstein	SD	Sudan		
DE	Germany	LK	Sri Lanka	SE	Sweden		
DK	Denmark	LR	Liberia	SG	Singapore		
EE	Estonia						

METHOD AND APPARATUS FOR ENHANCING ADHESION BETWEEN BARRIER LAYER AND METAL LAYER FORMED BY PLATING

Technical Field of the Invention

This invention relates to a method and apparatus for enhancing adhesion between barrier layer and metal layer formed by plating.

Background of the Invention

As semiconductor device feature continues to shrink according to the Moore's law, the interconnect delay is larger than device gate delay for 0.18 μm generation device if aluminum (Al) and SiO₂ is still being used. In order to reduce the interconnect delay, copper and low k dielectric are possible solution. Copper/low k interconnects provide several advantages over traditional Al/SiO₂ approaches, including the ability to significantly reduce the interconnect delay, while also reduce the number of level of metal required, minimizing power dissipation and reducing manufacturing costs. Copper offers improved reliability in that its resistance to electromigration is much better than aluminum's. A variety of techniques have been developed to deposit copper, ranging from traditional PVD and CVD techniques to new electroplating methods. PVD Cu associates with cusping problem, which results in void when filling small gap (<0.18 μm) with a large aspect ratio. The CVD Cu has high impurity incorporated inside the film during deposition, which needs a high temperature annealing to drive out the impurity in order to obtain a low resistivity Cu film. Only the *electroplating Cu* can provide both low resistivity and excellent gap filling capability at the same time. Another important factor is the cost, the cost of the *electroplating tool* is two third or half of that of *PVD* and *CVD tool*. Also, low process temperature (30 to 60 °C) of the electroplating Cu is mostly favored by low k dielectric (polymer, xerogels and aerogels) in succeeding generation of device.

Electroplating Cu have been used in printing board, bump plating in chip package, magnetic head industry for many years. In conventional plating machine, density of plating current flow to periphery of wafer is greater than that to center of wafer. This causes higher plating rate at periphery than at center of wafer. U.S. Pat. No. 4, 304,841 to Grandia et al. disclosed a diffuser being put between substrate and anode in order to obtain uniform plating current flow and electrolyte flow to substrate. U.S. Pat. No. 5,443,707 to Mori disclosed a method to manipulate plating current by shrinking the size of anode. U.S. Pat. No. 5,421,987 to Tzanavaras disclosed a rotation anode with multiple jet nozzles to obtain uniform and high plating rate. U.S. Pat. No. 5,670,034 to Lowery disclosed a transversely reciprocating anode in front of rotation wafer to improve plating thickness uniformity. U.S. Pat. No. 5,820,581 to Ang disclosed a thief ring powered by separate power supply to manipulate the plating current distribution across the wafer.

All those prior arts need Cu seed layer prior to the Cu plating. Usually the Cu seed layer is on the top of the diffusion barrier. This Cu seed layer is deposited either by physical vapor deposition (PVD), or chemical vapor deposition (CVD). As mentioned before, however, PVD Cu associates with cusping problem that results in void when filling small gap ($<0.18 \mu\text{m}$) with a large aspect ratio by succeeding Cu electroplating. The CVD Cu has high impurity incorporated inside the film during deposition, which needs a high temperature annealing to drive out the impurity in order to obtain a low resistivity Cu seed layer. As device feature size shrinks this Cu seed layer will become larger problem. Also, deposition of Cu seed layer adds additional process, which increases IC fabrication cost.

U.S. Pat. Application (Provision) No. 60/074,466 to Hui Wang disclosed a new innovative method and apparatus to plate metal (Copper) directly on barrier layer (TiN or TaN). It was found that the Cu can be plated on high resistive barrier layer without hydrogen being plated out, however, the adhesion between Cu and the TiN barrier layer is poor.

Summary of the Invention

It is an object of the invention to provide a novel method to enhance the adhesion between barrier layer and metal layer being plated.

It is a further object of the invention to enhance adhesion between barrier layer and the plated metal layer by pre-surface treatment.

It is an additional object of the invention to enhance adhesion between barrier layer and the plated metal layer by pre-surface treatment through plasma.

It is a further object of the invention to enhance adhesion between barrier layer and the plated metal layer by pre-surface treatment through ion irradiation.

It is a further object of the invention to enhance adhesion between barrier layer and the plated metal layer by pre-surface treatment through chemical vapor exposure.

It is a further object of the invention to enhance adhesion between barrier layer and the plated metal layer by pre-surface treatment through dipping into chemical liquid.

It is a further object of the invention to enhance adhesion between barrier layer and the plated metal layer by inserting a glue layer.

It is a further object of the invention to enhance adhesion between barrier layer and the plated metal layer by inserting a glue layer deposited through chemical vapor deposition (CVD).

It is a further object of the invention to enhance adhesion between barrier layer and the plated metal layer by inserting a glue layer deposited through physical vapor deposition (PVD).

It is a further object of the invention to enhance adhesion between barrier layer and the plated metal layer by inserting a glue layer deposited through the electroplating.

It is a further object of the invention to enhance adhesion between barrier layer and the plated metal layer by inserting a glue layer deposited through the electroless plating.

It is a further object of the invention to enhance adhesion between barrier layer and the plated metal layer by inserting a glue layer and surface treatment of the glue layer.

It is a further object of the invention to enhance adhesion between barrier layer and the plated metal layer by inserting a metal glue layer with electrode potential smaller than that of copper.

It is a further object of the invention to provide a plaiting system, which integrates plating module with surface treatment module.

It is a further object of the invention to provide a plaiting system, which integrates plating module with glue layer deposition module.

It is a further object of the invention to provide a plaiting system, which integrates plating module with both glue layer deposition module and surface treatment module.

Method 1: Pre-surface Treatment then Plating Metal Film

The above and other objects of the invention there are accomplished by the provision of a method for enhancing adhesion between barrier layer and the plated metal layer, comprising: 1) Performing pre-surface treatment to barrier layer by using

plasma, ion irradiation, chemical vapor exposure, or chemical liquid dipping; and 2) plating metal film on the treated surface; and 3) cleaning and drying the wafer.

Method 2: Glue Layer Deposition then Plating Metal Film

In the further aspect of the invention there is provided another method for enhancing adhesion between barrier layer and the plated metal layer, compromising: 1) depositing a glue layer on the barrier layer by using CVD method, PVD method, electroplating method, or electroless plating method; and 2) plating metal film on the glue layer; and 3) cleaning and drying the wafer.

Method 3: Glue Layer Deposition, Pre-surface Treatment, and then Plating Metal Film

In the further aspect of the invention there is provided another method for enhancing adhesion between barrier layer and the plated metal layer, compromising: 1) depositing a glue layer on the barrier layer by using CVD method, PVD method, electroplating method, immersion plating method, or electroless plating method; and 2) performing pre-surface treatment to the glue layer by using plasma, ion irradiation, chemical vapor exposure, or chemical vapor dipping; and 3) plating metal film on the treated glue layer; and 3) cleaning and drying the wafer.

Apparatus 1: Pre-surface Treatment Module combining with Plating Module and Cleaning/Drying Module

In the further aspect of the invention there is provided a apparatus for plating thin film directly on a substrate with a barrier layer on top, compromising: pre-surface treatment module; plating modules, cleaning/drying modules, wafer cassettes, wafer transferring system, and control hardware and software.

Apparatus 2: Glue Layer Deposition Module combining with Plating Module and Cleaning/Drying Module

In the further aspect of the invention there is provided another apparatus for plating thin film directly on a substrate with a barrier layer on top, compromising: glue layer deposition module; plating modules, cleaning/drying modules, wafer cassettes, wafer transferring system, and control hardware and software.

Apparatus 3: Glue Layer Deposition Module and Pre-surface Treatment Module combining with Plating Module and Cleaning/Drying Module

In the further aspect of the invention there is provided another apparatus for plating thin film directly on a substrate with a barrier layer on top, compromising: glue layer deposition module; pre-surface treatment module; plating modules, cleaning/drying modules, wafer cassettes, wafer transferring system, and control hardware and software.

BRIEF DESCRIPTION OF THE DRAWING

Fig. 1 shows a flow chart of process for enhancing adhesion through pre-surface treatment

Fig. 2 shows a block diagram of four kinds of pre-surface treatment methods

Fig. 3 shows a flow chart of process for enhancing adhesion through inserting a glue layer

Fig. 4 shows a block diagram of four kinds of methods to deposit glue layer on barrier layer.

Fig. 5 shows a flow chart of process for enhancing adhesion through inserting a glue layer and pre-surface treatment

Fig. 6 shows top and side cross-sectional views of plating system of this invention

DESCRIPTION OF PREFEED EMBODIMENT

1. Pre-surface Treatment

Fig. 1 shows process flow of enhancing adhesion through pre-surface treatment in accordance with the present invention. The pre-surface treatment is performed after barrier layer formation and prior to plating step. There are four types of pre-surface treatment as shown in Fig. 2.

Plasma Treatment

The surface of barrier layer can be activated through plasma exposure. For TiN, and TaN, gas for generating plasma can be chosen from SF₆, C₂F₃, Ar, and Cl₂. The central idea is to generate activation sites or dangling bond through physical and chemical bombardment on the surface. The bias voltage, plasma density, and exposure time can be varied to achieve high density of activation sites and lowest damage to barrier layer. Plasma sources can be chosen from low-pressure plasma, high-density plasma, and silent discharge plasma.

Example 1

Plasma source: low-pressure plasma source, pressure range 0.05 to 1 torr

Gas: Ar, flow range: 1 to 100 sccm; SF₆ range: 1 to 10 sccm

Plasma power: 100 Watts to 500 Watts

Treatment time: 10 seconds to 100 seconds.

Ion Irradiation

Similar to plasma treatment, the ion irradiation can be used to treat surface of the barrier layer. The ion can be chosen from, Ar⁺, Cl⁻, F⁻, N₂⁺, Cu⁺ and so on. The energy and flux can be varied to control the density of activation sites and damage range of barrier layer. The energy of ion should be in/under the range of sputtering threshold of atoms forming barrier layers.

Example 2

Ion source: Kaufman ion source

Ion: Cu⁺

Ion energy: 100 eV to 5000 eV;

Ion dose: 1xE14 to 1E19 ions/cm²

Irradiation vacuum: 1xE-4 to 1xE-8 Torr

Chemical Vapor Treatment

Instead of plasma and ion irradiation, chemical vapor also can be used to activate the surface of barrier layer. The central idea is to generate activation sites or dangling bond through chemical reaction or etching. Vapor can be chosen from HF, HCl, or any other chemicals, which can generate activation or nucleation sites on surface of barrier layer. The chemical vapor concentration, vapor flow speed, and exposure time are variables to control the nucleation density, surface etching rate. The objective is to activate surface without changing barrier layer either in property and physical dimension.

Example 3

Vapor: HCl

Vapor flow rate: 1 to 20 slm

Substrate temperature: 20 °C to 500 °C

Exposure time: 20 seconds to 200 seconds

Chemical Liquid Dipping

Instead of chemical vapor exposure, chemical liquid dipping can be used to activate the surface of barrier layer. Similarly, the objective is to generate activation sites or dangling bond through chemical reaction or etching. Chemicals can be chosen from HF, HCl, and any other chemicals, which can generate activation or nucleation sites on surface of barrier layer. The chemical concentration, solution flow speed, and dipping time are variables to control the nucleation density, surface etching rate.

Example 4

Chemical solution: HCl, 5 to 20%

Temperature of solution: 20 °C to 80 °C

Dipping time: 30 seconds to 10 minutes

Combination of above Methods

Barrier layer surface can be treated by combination of above methods for obtaining optima results. For instance, plasma treatment first, then chemical vapor exposure, or plasma treatment first, then chemical liquid dipping, or chemical exposure first, then plasma treatment, or chemical liquid dipping first, then ion irradiation.

2. Inserting Glue Layer

In order to enhance the adhesion between barrier layer and metal layer being plated, the glue layer can be inserted between the barrier layer and the metal layer. The glue layer itself has a good adhesion with both barrier layer and metal film. Most of glue layers are

selected from metals and their alloys. There are two category of glue layer described as follows.

Metals or Alloys having Lower Electrode Potential than that of Copper

The central idea is to use immersion plating to enhance the adhesion between the glue layer and copper. It is known that metal having a low electrode potential displaces a metal having a high electrode potential from its simple salt solution. For example, if a zinc piece is immersed in a solution of copper sulfate, it is noticed that the zinc is covered with a layer of copper metal. This is because that the electrode potential for Zinc is more negative than that for copper. This means copper has a greater tendency than copper to form ions in solution. The zinc atoms drive the copper ions out of solution to form metallic copper and the charges are transferred to the zinc atoms, which go into solution as zinc ions. Thus the reaction $Zn + Cu^{2+} = Zn^{2+} + Cu$ takes place. This process is also called immersion plating.

The process sequence is first to put a thin glue layer (less than 50 nm) on the barrier layer (for instance TiN) by using CVD method, PVD method, electroplating method, or electroless plating method as shown in Fig. 4. Then to dip the wafer into copper salt solution ($CuSiO_4 + H_2SiO_4$). The part of glue metal passes into solution and is replaced by Copper. The coatings are extremely thin (less than 25 nm) and can not be built up, since further displacement ceases once the substrate surface is covered with Cu. The standard electrode potentials of some metals are shown in following Table 1.

Table 1 Standard Electrode Potentials (In Volts)

Potassium (K^+)	-2.92	Iron (Fe^{3+})	-0.04
Sodium (Na^+)	-2.71	Hydrogen (H^+)	0.00
Magnesium (Mg^{2+})	-2.37	Tin (Sn^{4+})	+0.01
Aluminum (Al^{3+})	-1.67	Antimony (Sb^{3+})	+0.15
Manganese (Mn^{2+})	-1.18	Bismuth (Bi^{3+})	+0.20
Zinc (Zn^{2+})	-0.76	Copper (Cu^{2+})	+0.34
Chromium (Cr^{3+})	-0.74	Copper (Cu^+)	+0.52

Iron (Fe^{2+})	-0.44	Silver (Ag^+)	+0.80
Cadmium (Cd^{2+})	-0.40	Rhodium (Rh^{3+})	+0.80
Indium (In^{3+})	-0.34	Mercury (Hg^{2+})	+0.85
Cobalt (Co^{2+})	-0.28	Palladium (Pd^{2+})	+0.99
Nickel (Ni^{2+})	-0.25	Platinum (Pt^{2+})	+1.20
Tin (Sn^{2+})	-0.14	Gold (Au^{3+})	+1.50
Lead (Pb^{2+})	-0.13	Gold (Au^+)	+1.68

In principle, all metals having lower electrode potential than that of copper can be used to form glue layer; however, considering low resistivity, low diffusivity, Aluminum, Zinc, Nickel, Chromium, and their alloys with other metals are preferred.

Example 4

Glue layer: Ni, thickness of 20 nm, deposited by PVD.

Immersion plating solution: copper sulfate: 67 g/L, sulfuric acid: 170 g/L

Temperature: 20 °C to 15 °C

Immersion plating time: 10 to 100 seconds

Metal or Alloy having Higher Electrode Potential than that of Copper

The central idea is to put metal having higher electrode potential on barrier layer to enhance the adhesion between barrier layer and copper. The glue layer can be chosen from Silver, Rhodium, Palladium, Platinum, Titanium, Tantalum, Gold and their alloy. The glue layer deposition method can be CVD, PVD, electroplating, or electroless plating as shown in Fig. 4. The thickness of glue layer is in the range of 2 nm to 100 nm, and preferred 10 nm to 50 nm.

3. Glue Layer plus Pre-Surface Treatment

Some glue layers are easily oxidized or their surfaces are too smooth. In order to obtain good adhesion, the oxidized layer should be taken away and surface should be roughed prior to copper plating. For example, aluminum, stainless steel, and chromium have

theoretically negative electrode potential so should be capable of displacing copper metals readily. However, this does not occur. The reason is that these materials are usually covered with adherent and invisible oxide films that render the material effectively more noble. Even in non-immersion plating case, oxide film is not good for adhesion. For instance, Ti glue layer forms a oxide film, this oxide layer significantly degrade adhesion between copper and the Ti Glue layer. Also, surface roughness is another important factor to affect adhesion. Pre-surface treatment described in section 1 can be used here to take away oxide film and to rough the surface of glue layer. The process sequence is shown in Fig. 5.

Pre-surface treatment can be done in the same bath of plating. For instance, HCl can be added into sulfuric bath. HCl in the bath dissolves the TiO₂ film, after the virgin surface of Ti is formed, copper can be electroplated on the glue layer. Also, alkali present chemically dissolves the aluminum oxide film, as soon as the virgin surface of aluminum is formed, immersion copper deposition begins.

Example 5

Glue layer: 20 nm Ni deposited by PVD

Dipping liquid: 5 to 20% HCl

Dipping time: 1 to 10 minutes

Dipping liquid temperature: 20 °C to 80 °C

Example 6

Glue layer: 20 nm Ti deposited by PVD

Dipping liquid: 5 to 20% HCl

Dipping time: 1 to 10 minutes

Dipping liquid temperature: 20 °C to 80 °C

4. System Architecture Design (Stacked Structure)

Fig. 6 is a schematic view of one embodiment of the plating system for plating conductive film on semiconductor wafer in accordance with the present invention. It is a stand-alone, fully computer controlled system with automatic wafer transfer, cleaning module with wafer dry-in and dry-out capability. It consists of one stacked glue layer deposition chamber 310, one stacked pre-surface treatment chamber 312, five stacked plating baths 300, 302, 304, 306, 308, three stacked cleaning/dry chambers 314, 316, 318, robot 322, wafer cassette 321, 322, electrolyte tank 36 and plumbing box 330. Plating bath 300 consists of anodes, power supplies, cylindrical wall or tube, wafer chuck, driving means to rotating or oscillating wafer during plating process. Electrolyte tank 36 includes temperature control set. Plumbing box 330 consists of pump, LMFCs, valves, filter, and plumbing. The plating system further consists of computer control hardware, and operation software package. Operation process sequence is described as follows:

Wafer plating operation sequence

Step A: Load wafer cassette 320, 321 by manual or robot.

Step B: Select recipe and push run button

Step C: Control software start to initialize the system including checking all system parameters within specification, and no any alarm existing in the system.

Step D: After completing the initialization, robot 322 picks up a wafer from cassette 320 or 321 and send to glue layer deposition chamber 310.

Step E: Deposit glue layer on the wafer

Step F: After finishing deposition, robot 322 pick up the deposited wafer from the chamber 310, and transport it to pre-surface treatment chamber 312.

Step G: Perform surface treatment on the glue layer.

Step H: After finishing surface treatment, robot 322 pick up the wafer from the chamber 312, and transport it to one of plating bathes (300, 302, 304, 306, or 308).

Step I: Perform plating

Step J: After finishing plating, robot 322 pick up the plated wafer from the plating bath, and transport it to one of cleaning/drying chamber (314, 316, or 318)

Step K: Cleaning the plated wafer.

Step L: Dry the plated wafer through spin-fry and/or N₂ purge

Step M: Robot 322 picks up the dried wafer and transport to cassette 320 or 321.

In Fig. 6, glue layer deposition chamber 310 can be CVD chamber, PVD chamber, electroplating chamber, or electroless plating chamber. Also pre-treatment chamber can be plasma treatment chamber, ion irradiation chamber, chemical vapor exposure chamber, or chemical liquid dipping chamber.

Also in above system, either glue layer deposition chamber or pre-surface treatment chamber can be eliminated., i.e. system consists of the glue layer deposition module, the plating module and the cleaning/drying module, or consists of pre-surface treatment module, plating modules and cleaning/drying module.

Instead of copper, the plating metal can be Silver, Aluminum, Gold, and their alloy with other metal. Plating metal also can be any other metal and alloy which can be used to form interconnector in IC chip.

Plating mentioned above can be electroplating, or electroless plating.

It should be further apparent to those skilled in the art that various changes from and details of the invention as shown and described may be made. It is intended that such changes be included within the spirit and scope of the claims appended hereto.

What is claimed is:

1. A method for enhancing adhesion between barrier layer and metal layer formed by the plating, comprising:
 - performing pre-surface treatment on barrier layer; and
 - plating metal film on the treated surface.
2. The method of claim 1 in which the pre-surface treatment is plasma exposure.
3. The method of claim 2 in which the plasma is generated by gases of SF₆, C₂F₅, Ar, Cl₂, or N₂.
4. The method of claim 1 in which the pre-surface treatment is ion irradiation
5. The method of claim 4 in which the ions are chosen from Ar⁺, Cl⁻, F⁻, N₂⁺.
6. The method of claim 1 in which the pre-surface treatment is chemical vapor exposure.
7. The method of claim 6 in which the chemical vapor is chosen from HF, or HCl vapor, or the combination of both HF and HCl.
8. The method of claim 1 in which the pre-surface treatment is chemical liquid dipping.
9. The method of claim 8 in which the chemical liquid is chosen from HF, or HCl liquid, or the combination of both HF and HCl liquid.
10. The method of claim 1 in which the plating method is the electroplating.
11. The method of claim 1 in which the metal film is copper film.

12. The method of claim 1 further compromises a step of cleaning and drying wafer after plating the wafer.
13. A method for enhancing adhesion between barrier layer and metal layer formed by the plating, comprising:
 - depositing a glue layer on the barrier layer; and
 - plating metal film on the glue layer.
14. The method of claim 13 in which the glue layer is deposited by using CVD method.
15. The method of claim 13 in which the glue layer is deposited by using PVD method.
16. The method of claim 13 in which the glue layer is deposited by using the electroplating method.
17. The method of claim 13 in which the glue layer is deposited by using the electroless plating method.
18. The method of claim 13 in which the glue layer is deposited by using the immersion plating method.
19. The method of claim 13 further compromises a step of cleaning and drying wafer after plating the wafer.
20. A method for enhancing adhesion between barrier layer and metal layer formed by the plating, comprising:
 - depositing a glue layer on the barrier layer; and
 - performing pre-surface treatment on barrier layer; and
 - plating metal film on the glue layer.

21. The method of claim 20 further compromises a step of cleaning and drying wafer after plating the wafer.
22. An apparatus for plating thin film directly on a substrate with a barrier layer on top, comprising:
 - a pre-surface treatment module; and
 - a plating module; and
 - a cleaning/drying module
23. The apparatus of claim 22 further comprises a wafer cassette, a wafer transferring system, and a control hardware and software.
24. An apparatus for plating thin film directly on a substrate with a barrier layer on top, comprising:
 - a glue layer deposition module; and
 - a plating module; and
 - a cleaning/drying module
25. The apparatus of claim 24 further comprises a wafer cassette, a wafer transferring system, and a control hardware and software.
26. An apparatus for plating thin film directly on a substrate with a barrier layer on top, comprising:
 - a glue layer deposition module; and
 - a pre-surface treatment module; and
 - a plating module; and
 - a cleaning/drying module

27. The apparatus of claim 26 further comprises a wafer cassette, a wafer transferring system, and a control hardware and software.

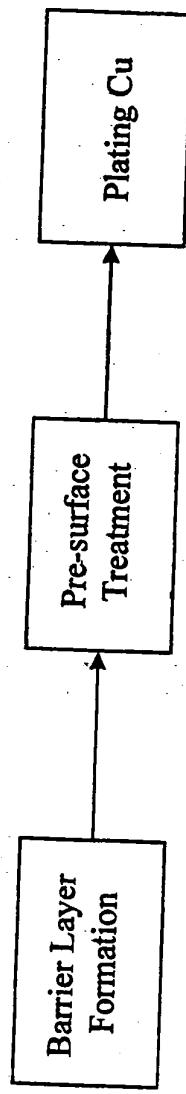


Fig. 1

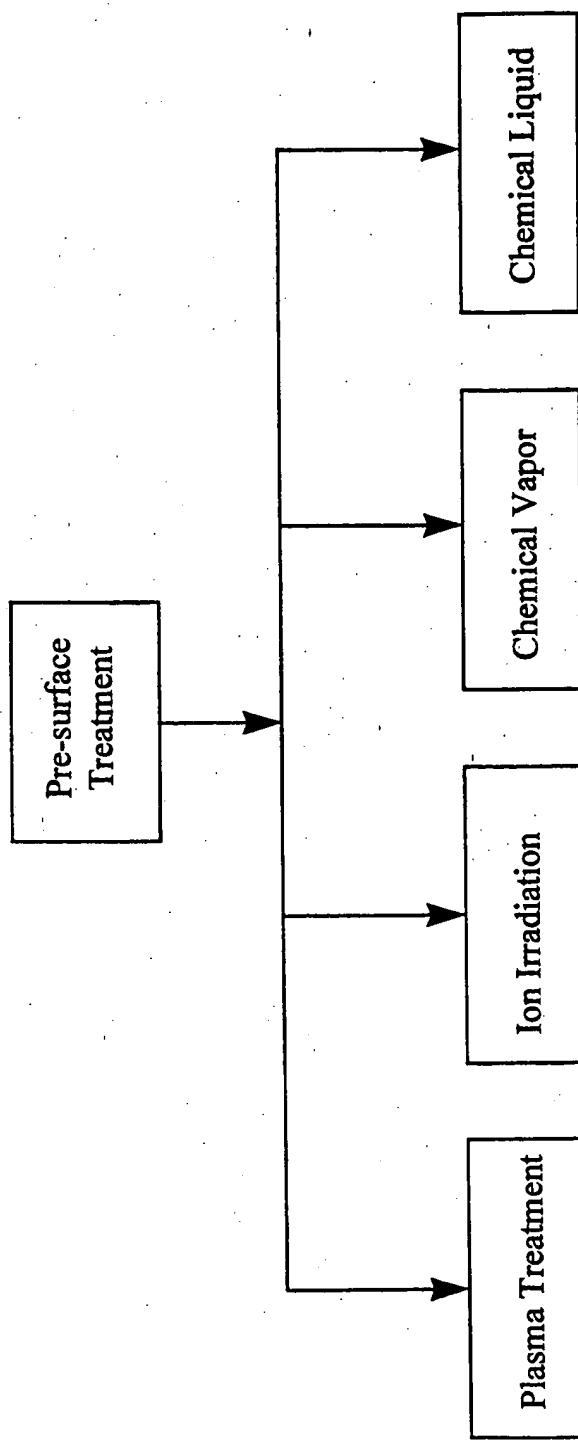


Fig. 2

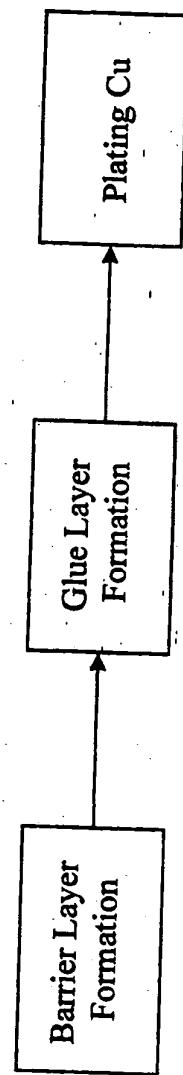


Fig. 3

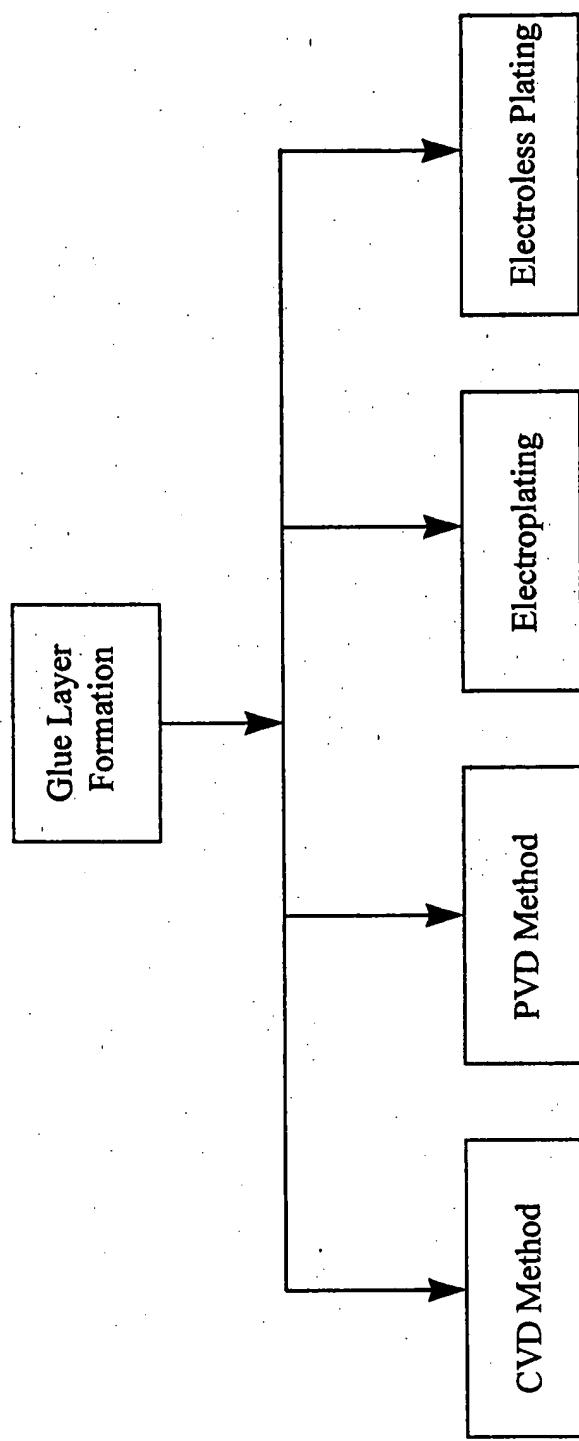


Fig. 4

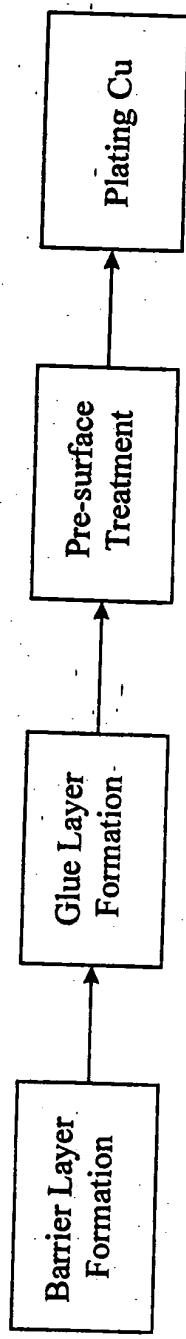


Fig. 5

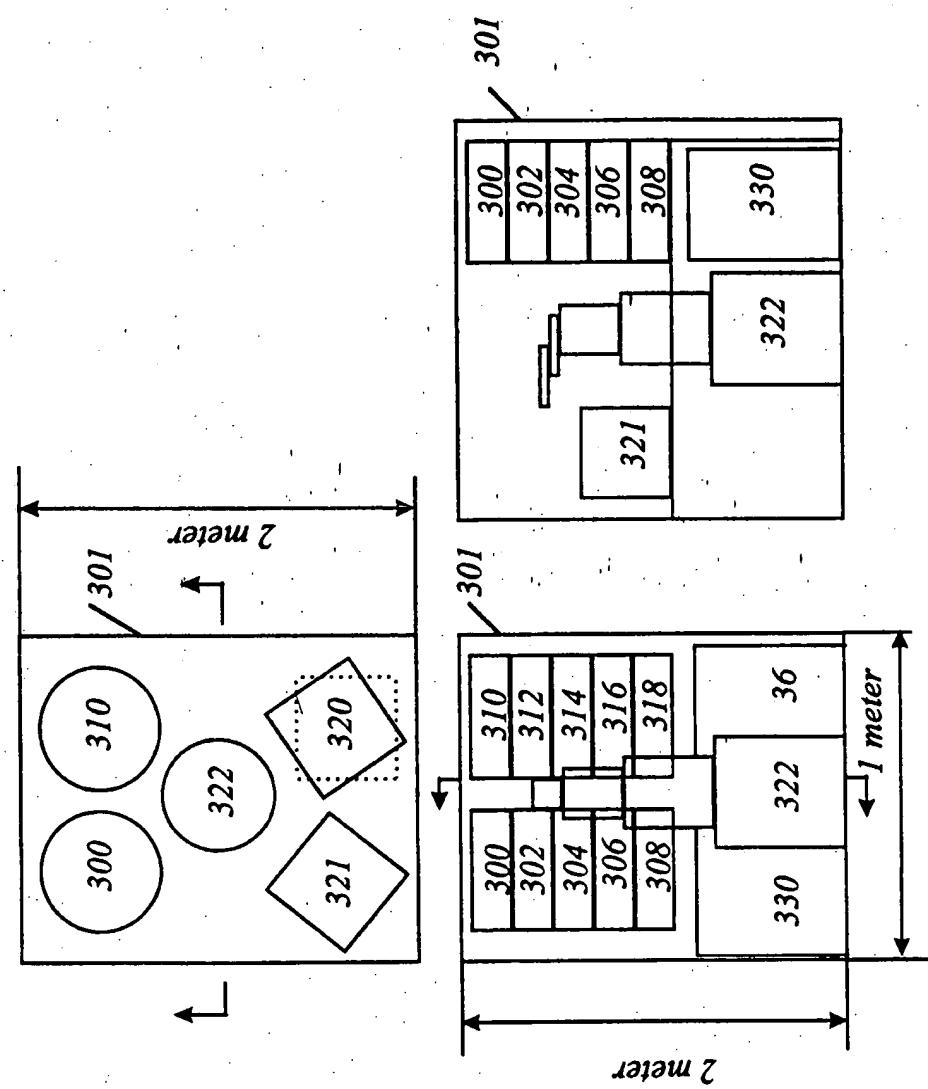


Fig. 6

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/07906

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 C23C18/18 C25D5/34 H01L21/288

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 C23C C25D H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 723 028 A (PORIS JAIME) 3 March 1998 (1998-03-03) the whole document	1,10,11, 13,15, 24,25
X	WO 97 22419 A (OBERLE ROBERT R) 26 June 1997 (1997-06-26)	1,8,9, 11,13, 18,20, 14
A	page 3, line 11 - page 7, line 20	
X	EP 0 510 711 A (CALVERT JEFFREY M ET AL) 28 October 1992 (1992-10-28) page 3, line 46 - page 5, line 25; examples 21,23	1,2,4,6, 8,11-13, 19
		-/-

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier document but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

Date of mailing of the international search report

29 July 1999

09/08/1999

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl.
Fax: (+31-70) 340-3016

Authorized officer

Köpf, C

INTERNATIONAL SEARCH REPORT

Inte	onal Application No
PCT/US 99/07906	

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	BRUNI M D: "THE ELECTROLESS CATALYTIC PROPERTIES OF AN EFFICIENT CR BASED BARRIER FOR CU DIFFUSION" EXTENDED ABSTRACTS, vol. 93/2, 1 January 1993 (1993-01-01), page 868/869 XP000422428 ISSN: 0160-4619 the whole document ---	1-3, 6, 11
X	EP 0 341 546 A (LINKA GERD ET AL) 15 November 1989 (1989-11-15) the whole document ---	1, 8-10, 13, 17, 20
E	EP 0 903 774 A (HONGO AKIHISA ET AL) 24 March 1999 (1999-03-24) paragraph '0030! - paragraph '0037! ---	22, 23
A	WEBER A ET AL: "ELECTROPLATING OF POLY(TETRAFLUOROETHYLENE) USING PLASMA ENHANCED CHEMICAL VAPOR DEPOSITED TITANIUM NITRIDE AS AN INTERLAYER" APPLIED PHYSICS LETTERS, vol. 67, no. 16, 16 October 1995 (1995-10-16), pages 2311-2313, XP000544365 ISSN: 0003-6951 the whole document ---	1, 2, 4, 5, 8, 10, 11, 13, 17

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte onal Application No

PCT/US 99/07906

Patent document cited in search report	Publication date		Patent family member(s)	Publication date
US 5723028 A	03-03-1998	US	5368711 A	29-11-1994
		US	5256274 A	26-10-1993
WO 9722419 A	26-06-1997	AU	1150397 A	14-07-1997
		CA	2238490 A	26-06-1997
		EP	0866735 A	30-09-1998
EP 0510711 A	28-10-1992	JP	5202483 A	10-08-1993
		US	5389496 A	14-02-1995
		US	5500315 A	19-03-1996
		US	5648201 A	15-07-1997
EP 0341546 A	15-11-1989	DE	3816495 A	23-11-1989
		JP	2070073 A	08-03-1990
EP 0903774 A	24-03-1999		NONE	